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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,046	08/03/2001	Nai-Shung Chang	JCLA6385	7558

7590 08/31/2004

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EXAMINER	
VO, TIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/922,046	CHANG, NAI-SHUNG	
	Examiner	Art Unit	
	Tim T. Vo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-15 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 are rejected under 35 U.S.C. § **102(b)** as being anticipated by Horan et al. patent number 5,892,964.

As for claim 1, Horan teaches an extended bus structure, for coupling with a control chip set, the control chip set also coupled with a central processing, a system memory, and a bus, the extended bus structure comprising (figure 4A,core logic 104 (control chip set) coupled with CPU 12, RAM 106 (system memory), and a bus 103, 104, 109), comprising:

a first accelerated graphics port bus, for coupling with the control chip set (see figure 4a, AGP bus 302 coupling to the core logic 104 and column 12 line 66 to column 13 line 10 and column 12 line 66 to column 13 line 10);

a first extended bus for expanding the first accelerated graphics port bus (see figure 4a, AGP bus 304 and column 12 line 66 to column 13 line 10);

a first bridge coupled to the first accelerated graphics port bus and the first extended bus for converting mutually and compatibly signal and data between the first accelerated graphics port bus and first extended bus (see figure 4a, core logic 104, coupling to the first AGP bus 302 and the first extended AGP bus 304. Column 9 line 65 to column 10 line 4, Horan teaches the core logic chip 104 comprising a bridge. Further, column 12 line 66 to column 13 line 35, Horan teaches the bridge for coupling buses 302, 304 and they are compatible to each other for data transfer between each other (column 4 line 66 to column 5 line 2).

As for claims 2, 10 and 13, Horan teaches the first bridge comprising a main accelerated graphics controller coupled to the first accelerated graphics bus compatibility receiving and transmitting data and signal thereof (see figure 3, bridge 104, receiving and transmitting data and signals to buses 302, 304);

a first extended bus controller coupled to the first extended bus for compatibility receiving and transmitting data and signal thereof (see figure 3, bus controller AGP 216 receiving and transmitting data to APG bus 304); and

a flow controller coupled to the main accelerated graphics port controller and the first extended bus controller for arbitrating and controlling flow direction of data and signal of the main accelerated graphics port controller and the first extended bus controller (see figure 3, AGP controller 210b, arbiter 216 and column 13 lines 8-10).

As for claims 3, 6 Horan teaches a second accelerated graphics port bus coupled to the first bridge to expand the first accelerated graphics port bus, wherein data and signal of the first and second accelerated graphics port buses are mutually and

compatibility converted by the first bridge (see figure 3, AGP controller 210a, arbiter 216 and column 13 lines 8-10).

As for claims 4, 7, 11 and 14, Horan teaches a main accelerated graphics port controller coupled to the first accelerated graphic port bus for compatibility receiving and transmitting data and signal thereof (see figure 3, main controller 218a);

first extended bus controller for arbitrating and controlling flow direction of data and signal of the main accelerated graphics port controller and the first extended bus controller (see figure 3, AGP controller 210b, arbiter 216 and column 13 lines 8-10).

an extended accelerated graphics port controller coupled to the second accelerated graphics port bus for compatibility receiving and transmitting data and signal of the second accelerated graphics port bus (see figure 3, the bus on the left of bus 211, this bus provides connection to other AGP controller);

a flow controller coupled to the main accelerated graphics port controller, the extended accelerated graphic port controller, and the first extended bus controller for arbitrating and controlling flow direction of data and signal of the main accelerated graphics port controller, the extended accelerated graphics port controller, and the first extended bus controller (see figure 3, AGP controllers 210a,b, arbiter 216).

As for claims 5, 12 and 15, Horan teaches a second extended bus to expand the second accelerated graphics port bus (see figure 3, PCI bus); and a second bridge coupled to the second accelerated graphic ports bus and the second extended bus for converting mutually and compatibility data and signal of the second accelerated graphics port bus and the second extended bus (see figure 3, PCI bridge).

As for claims 8-9, Horan teaches a control chip set coupled to the first accelerated graphics port bus, a peripheral coupled to the first extended bus (see figure 3).

Response to Arguments

1. Applicant's arguments filed 06/10/04 have been fully considered but they are not persuasive.

2. In response to the applicant's arguments that Horan fails to disclose an additional bridge coupled between the original AGP bus and an extended bus as claimed in independent claims 1, 10 and 13. Examiner referred the core logic 104 comprising a bridge to connect AGP buses 302, 304 as disclosed in figure 4A and column 9 line 65 to column 10 line 4.

3. In response to the applicant's arguments that the AGP buses 302, 304 are directly coupled to the logic chip set 218 and the current invention does not, wherein figure 2 discloses the bridge 230 is not directly coupled to the control chip set. This argument is moot because the claim's language fails to particularly point out and distinctly from Horan. For example, the preamble indicates "An extended bus structure, for coupling with a control chip set, the control chip set also coupled with a central processing, a system memory, and a bus, the extended bus structure comprising:". As pointed out above in the office action, figure 4A of Horan anticipates these features i.e. the core logic 104 (control chip set) coupled with CPU 12, RAM 106 (system memory), and a bus 103, 104, 109. Further, the claim's language indicates "a first accelerated graphics port bus, for coupling with the control chip set". Again figure 4A anticipates

these limitations i.e. AGP bus 302 coupling to the core logic 104 and column 12 line 66 to column 13 line 10). Last but not least the claim indicates "a first bridge coupled to the first accelerated graphics port bus and the first extended bus for converting mutually and compatibly signal and data between the first accelerated graphics port bus and first extended bus". Figure 4A anticipates these limitations i.e. wherein a bridge located within the core logic 104 for connecting 2 or more AGP buses and they are compatible to each other column 4 line 66 to column 5 line 2. This is equivalent to what is claimed.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

08/26/04

Tim T. Vo
Primary Examiner
Art Unit 2112